Amendments to the Claims:

Please delete claims 1-5 and 7-8 without prejudice to reinstate, amend claims 25-30, 35, 40 and 44 and add new claims 53-59 as follows:

Claims 1-23 Canceled

24. (Previously Presented) An interface, comprising:

a circuit adapted to couple to a first bus having parallel bus data, the circuit adapted to serially send the bus data over a link to a physically remote second bus without requiring or waiting for an incoming acknowledgement over the link before inaugurating a transfer of the serialized bus data over the link.

25. (Currently Amended) The interface ~~bridge~~ according to claim 24 wherein the first bus is a PCI-type bus.

26. (Currently Amended) The interface ~~bridge~~ according to claim 24 wherein the circuit is an integrated circuit.

27. (Currently Amended) The interface ~~bridge~~ according to claim 26 wherein the integrated circuit is an application specific integrated circuit (ASIC).

28. (Currently Amended) The interface ~~bridge~~ according to claim 24 wherein the circuit is operable to exchange bus data according to a predetermined hierarchy giving the first bus a higher level than the second bus.

29. (Currently Amended) The interface ~~bridge~~ according to claim 24 further comprising a first register adapted to hold parallel bus data.

30. (Currently Amended) The interface ~~bridge~~ according to Claim 29 further comprising a second register adapted to hold received second bus data.

31. (Previously Presented) A bridge accessible by a processor for expanding access over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, said bridge comprising:

a link;

a first interface coupled between said first bus and said link; and

a second interface adapted to couple between said second bus and said link, said first interface and said second interface being operable to transfer bus data serially through said link without waiting for an incoming acknowledgment over said link before inaugurating a transfer of said bus information over said link.

32. (Previously Presented) The bridge according to claim 31 wherein said first interface and said second interface are operable to exchange information between said first bus and said second bus according to a predetermined hierarchy giving said first bus a higher level than said second bus.

33. (Previously Presented) The bridge according to claim 31 wherein said first bus and said second bus each have a plurality of signaling lines for enabling bus-compatible devices to negotiate bus communications, said first interface being operable in response to a pending transaction on said first bus to begin processing said pending transaction and to apply a retry

signal to at least one of said signaling lines of said first bus before the pending transaction on said first bus has been transmitted to and acknowledged by said second bus.

34. (Previously Presented) The bridge according to claim 33 wherein less than all of the information on the signaling lines of said first bus is transmitted by said first interface over said link.

35. (Currently Amended) The bridge according to claim 31 wherein said first interface is selectively responsive to ~~those~~ addresses appearing on said first bus that are on a predetermined schedule of addresses corresponding to the bus-compatible devices accessible through said second bus, in order to avoid responding to addresses corresponding to other ones of the bus-compatible devices on said first bus.

36. (Previously Presented) The bridge according to claim 35 comprising:

a register for storing said predetermined schedule.

37. (Previously Presented) The bridge according to claim 35 wherein said first interface comprises:

a first register for storing said predetermined schedule, said second interface comprising:

a second register for storing said predetermined schedule.

38. (Previously Presented) The bridge according to claim 36 wherein said register is operable to establish with respect to said first bus a base address for one or more of the bus-compatible devices on said second bus.

39. (Previously Presented) The bridge according to claim 31 comprising:

a register for establishing with respect to said first bus a base address for one or more of the bus-compatible devices on said second bus.

40. (Currently Amended) The bridge according to claim 31 wherein said first interface and said secondary interface are operable to permit communication between bus-compatible devices on said second bus without routing through said first bus.

41. (Previously Presented) The bridge according to claim 31 wherein said first interface and said second interface comprise:

a first and a second programmable logic device connected between said link and said first bus and said second bus, respectively.

42. (Previously Presented) The bridge according to claim 31 wherein said first interface and said second interface comprise:

a first and a second application-specific integrated circuit connected between said link and said first bus and said second bus, respectively.

43. (Previously Presented) The bridge according to claim 42 wherein said first and said second application-specific integrated circuit are identically structured and each have a control pin for receiving a control signal to establish operation in one of two modes.

44. (Currently Amended) The bridge according to claim 42 wherein said first and said second application-specific integrated circuit each comprise:

a plurality of ports ~~coupled to said second interface for providing~~ configured to provide input/output of the bus data.

45. (Previously Presented) The bridge according to claim 31 wherein said processor is interrupt-driven, said second interface being operable to transmit through said link to said first interface interrupt signals destined to interrupt the processor.

46. (Previously Presented) The bridge according to claim 45 wherein said processor is responsive to error signals, said second interface being operable to transmit through said link to said first interface error signals destined to affect the processor.

47. (Previously Presented) The bridge according to claim 31 wherein said first bus operates at a predetermined clock speed, said link being operable to propagate data between said first interface and said second interface at a bit transfer rate greater than said predetermined clock speed.

48. (Previously Presented) The bridge according to claim 47 wherein said link comprises:

a pair of simplex links for sending information in opposite directions.

49. (Previously Presented) The bridge according to claim 48 wherein said simplex links are driven for differential signal transfers.

50. (Previously Presented) The bridge according to claim 31 wherein said second bus comprises a PCI bus.

51. (Previously Presented) The bridge according to claim 31 wherein said second interface is operable in response to a transaction from said link signifying an initial read request, to fetch and pre-fetch data from a competent one of the bus-compatible devices on said second bus for transmission back over said link in order to satisfy pending and anticipated transactions.

52. (Previously Presented) The bridge according to claim 31 wherein said first interface and said second interface are operable to permit at least one of the bus-compatible devices on said second bus to address one or more of the bus-compatible devices on said first bus using on said second bus substantially the same type of addressing as is used to access devices on said second bus.

53. (New) A bridge for expanding access, over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, said bridge comprising:

a link;

a first interface adapted to couple between said first bus and said link;

and

a second interface adapted to couple between said second bus and said link, said first interface and said second interface operating as a bridge and being operable to transfer information serially through said link in a format different from that of said first bus and said second bus without waiting for an incoming acknowledgement over said link before inaugurating a transfer of said information over said link;

characterized in that during a transaction the information provided to the first interface is tagged with data indicative of the transaction type and the information is transferred from the first interface to the second interface without waiting for an incoming acknowledgement from the second interface before inaugurating a transfer of said information over said link.

54. (New) The bridge according to claim 53 wherein the first interface and the second interface each comprise a register, wherein the information provided to the first interface is loaded into the first register and mirrored to the second register.

55. (New) A bridge according to claim 53 wherein said allowable ones of said bus-compatible devices include memory devices and input/output devices, said first interface and said second interface being operable to (a) approve an initial exchange between said first bus and said second bus, in response to pending bus transactions having a characteristic signifying a destination across said bridge, and (b) allow communications to be addressed individually through said first bus, to different selectable ones of the bus-compatible devices on said second bus, including memory devices and input/output devices that may be present: (i) using on said first bus substantially the same type of addressing as is used to access devices on said first bus, and (ii) without first employing a second, intervening one of the bus-compatible devices on said second bus.

56. (New) A bridge according to claim 53 wherein said first interface and said second interface are operable to exchange information between said first bus and said second bus according to a predetermined hierarchy giving said first bus a higher level than said second bus.

57. (New) A bridge according to claim 53 wherein said first interface and said second interface are operable to (a) exchange information between said first bus and said second bus according to a predetermined hierarchy giving said first bus a higher level than said second bus, and (b) allow communications to be addressed individually through said first bus, to different selectable ones of the bus-compatible devices on said second bus, including memory devices and input/output devices that may be present: (i) using on said first bus substantially the same type of addressing as is used to access devices on said first bus, (ii) without first employing a second, intervening one of the bus-compatible devices on said second bus, and (iii) without passing the information through an intervening hierarchical level.

58. (New) A bridge according to claim 53, wherein said first bus and said second bus each have a plurality of signaling lines for enabling bus-compatible devices to negotiate bus communications, said first interface being operable in response to a pending transaction on said first bus to begin processing said pending transaction and to apply a retry signal to at least one of said signaling lines of said first bus before the pending transaction on said first bus has been transmitted to and acknowledged by said second bus.

59. (New) A bridge according to claim 53 wherein less than all of the information on the signaling lines of said first bus is transmitted by said first interface over said link.